

REMARKS

Claims remaining in the present patent application are Claims 1-8 and 21-28. The Applicants respectfully request reconsideration of the above captioned patent application in view of the remarks presented herein.

Drawings

The drawings are objected to under 37 CFR § 1.83(b) and 37 CFR § 1.84(p)(5).

Applicants respectfully assert that the original drawings and the description thereof appearing in the specification fully describe the present claimed embodiments and would be readily understood by one of ordinary skill in the art. Applicants respectfully assert that the original drawings fully comply with 37 CFR § 1.21(d), 37 CFR § 1.83(b) and 37 CFR § 1.84(p)(5).

In the interests of advancing prosecution, Applicants submit an amended drawing sheet to further clarify the disclosure. Applicants respectfully assert that no new matter is added as a result of these drawing amendments. Applicants respectfully solicit withdrawal of the drawing objections.

35 U.S.C. § 102

Claims 1-8 and 21-28 stand rejected under 35 U.S.C. § 102(b) as being allegedly unpatentable over Rastegar et al. (US 5,422,591, “Rastegar”). Applicants have carefully reviewed the cited reference and respectfully assert that embodiments of the present invention as recited in Claims 1-8 and 21-28 are patentable over Rastegar.

Claims 1 and 21 recite the claimed limitation, “wherein said switch is operable to selectively couple said second input to said output terminal responsive to a voltage of said substrate bias supply line.” The rejection proposes that the line attached to node C is analogous to the recited “substrate bias supply line.” Applicants note this line is illustrated as an output (arrow pointing out) in Rastegar Figure 2. The rejection also recognizes this function, describing “output terminal C.” Hence, terminal C is an output terminal, and no control function is ascribed.

Substituting the rejection’s construction, the instant limitation would read, “wherein said switch is operable to selectively couple said second input to said output terminal responsive to a voltage of said (output terminal C).” Rastegar does not teach any control function to terminal C, an output. Thus, the Rastegar switch is not operable to connect anything responsive to “a voltage

of said substrate bias supply line” as recited by Claim 1. Consequently, Rastegar fails to teach or suggest at least this claimed limitation.

For this reason, Applicants respectfully assert that Claims 1 and 21 overcome the rejections of record, and respectfully solicit allowance of these Claims.

In addition with respect to Claims 1 and 21, Applicants respectfully assert that Rastegar fails to teach or suggest the claimed limitation of “a second input for controlling said switch,” as recited by Claims 1 and 21. The rejection alleges that terminals A and B teach the recited first and second inputs for controlling said switch. Applicants respectfully traverse. Regardless of whether terminal A or B suggests the first input for controlling said switch, Rastegar fails to teach or suggest a second input for controlling switch 30. Input A is the only taught control input. As taught by Rastegar, either terminal B or D is coupled to terminal C, based only on the voltage at terminal A (column 4, lines 2-39). No other terminal is taught as having a capability to control switch 30. Thus, Rastegar teaches a single control input, and fails to teach or suggest a second input for controlling said switch, as recited by Claims 1 and 21.

For this additional reason, Applicants respectfully assert that Claims 1 and 21 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that the rejection mischaracterizes the function of switch 30. For example, the rejection alleges that “said switch is capable, in fact: configured, to selectively couple said second input A to said output terminal C....” Applicants do not find such teaching in the cited art. For example, Rastegar teaches, “When reading a high signal at A, control 30 connects node 20 input at B to the well-tie of transistor Q1 through C” (column 4 lines 2-4). Thus, Rastegar teaches a connection between nodes B and C, but no coupling between A and any other node. Further, Rastegar teaches, “A low signal N1out at A causes control 30 to switch the body bias connection of transistor Q1 at C to ground at D” (column 4 lines 20-22). Herein, Rastegar teaches a connection between nodes D and C, but no coupling between A and any other node. Thus, the rejection’s allegation of coupling involving terminal A is not supported by the art.

Further with respect to Claims 1 and 21, Applicants respectfully assert that Rastegar fails to teach or suggest the claimed limitation of “a second input for controlling said switch coupled to a substrate bias supply line,” as recited by Claims 1 and 21. As terminal A is the only line taught by Rastegar to control a

switch, and terminal A is not “coupled to a substrate bias supply line,” as recited by Claims 1 and 21, no line or terminal described by Rastegar suggests a single line that both controls the switch and is coupled to a substrate bias supply line, as claimed in this recited limitation.

For this further reason, Applicants respectfully assert that Claims 1 and 21 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that Claims 2-8 and 22-28 overcome the rejections of record by virtue of their dependence, and respectfully solicit allowance of these Claims.

CONCLUSION

Claims remaining in the present patent application are Claims 1-8 and 21-28. The Applicants respectfully request reconsideration of the above captioned patent application in view of the remarks presented herein.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 504160.

Respectfully submitted,

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